# DESIGN AND SIMULATION OF WLAN (802.11a) TRANSMITTER

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**ABSTRACT-**The growth of 802.11based wireless LANs provides higher data rates and greater system capacities. Among the IEEE 802.11 standards, the 802.11a standard based on OFDM modulation scheme has been defined for high-speed and large-system-capacity challenges. Orthogonal Frequency Division Multiplexing (OFDM) has been selected as the modulation scheme due to its good performance on highly dispersive channels, like the indoor scenarios where these standards will be used. The IEEE802.11a standard supports 6, 9, 12, 18,24,36,48 and 54Mbps data rates. Out of these eight data rates, 6, 12 and 24Mbps are mandatory data rates. In this paper VHDL design of the physical layer of IEEE802.11a standard for 6Mbps data rate is presented. The PHY of IEEE 802.11a is first simulated using MathWorks Simulink and then Implementation aspects of an OFDM modem on Xilinx FPGA are addressed. The system includes simulation of Data Scrambler, convolutional encoder, data Interleaver, BPSK modulator and 64 point IFFT. The design is efficiently synthesized on Virtex xqv600e-6bg432.

**Index Terms**— WLAN, OFDM, SIMULINK, VHDL,FPGA, Virtex, IEEE802.11a.

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## I. INTRODUCTION

Wireless technology has helped to simplify networking by enabling multiple computer users to simultaneously share resources in a home or business without additional or intrusive wiring. These resources include a broadband Internet connection, data files, network printers, and even streaming audio and video [1]. This kind of resource sharing has become important as computer users have changed their habits from using single, stand-alone computers to working on networks with multiple computers, each with different operating systems and varying peripheral hardware. Components that can connect into a wireless medium in a network are called as stations. All stations are equipped with wireless network interface controllers (WNICs). Wireless stations fall into one of two categories:access points, and clients.

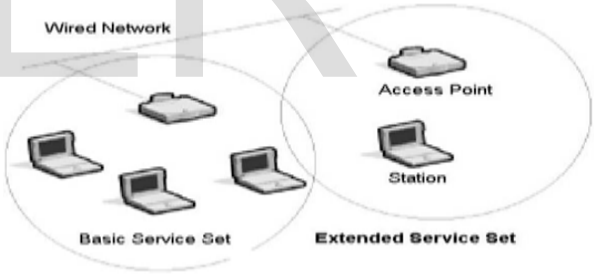


Fig. 1 WLAN Architecture

Access points (APs), normally routers, are base stations for the wireless network. They transmit and receive radio frequencies for wireless enabled devices to communicate with. Wireless clients can be mobile devices such as laptops, IP phones, personal digital assistants and other smartphones, or fixed devices such as desktops and workstations that are equipped with a wireless network interface. The basic service set (BSS) is a set of all stations that can communicate with each other. There are two types of BSS: Independent BSS (also referred to as IBSS), and infrastructure BSS. Every BSS has an identification (ID) called the BSSID, which is the MAC address of the access point servicing the BSS. An independent BSS (IBSS) is an ad-hoc network that contains no access points, which means they cannot connect to any other basic service set.

An infrastructure can communicate with other stations not in the same basic service set by communicating through access points. An extended service set (ESS) is a set of connected BSSs. Access points in an ESS are connected by a distribution system. Each ESS has an ID called the SSID which is a 32-byte (maximum) character string. A distribution system (DS) connects access points in an extended service set. The concept of a DS can be used to increase network coverage through roaming between cells. DS can be wired or wireless. Current wireless distribution systems are mostly based on WDS or MESH protocols, though other systems are in use. This paper is organized as follows section II discusses the WLAN types. In section III, detailed block diagram with description for WLAN 802.11a is presented. Section IV emphasize on implementation of WLAN (802.11a) transmitter using xilinx. Section V, firstly simulation results using mathworks simulink are given and then synthesis and simulation results on Virtex xqv600e-6bg432 are presented. Finally the paper is concluded in section VI.

## II. WLAN TYPES

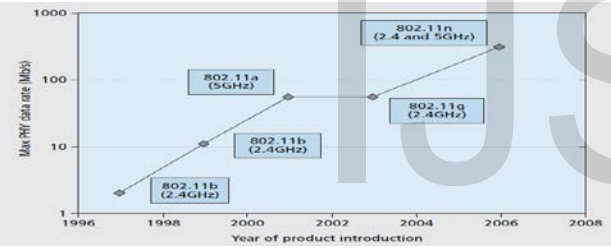


Fig 2. WLAN Evolution [8]

The Institute of Electrical and Electronic Engineers (IEEE) released the 802.11 specifications in June 1999. The initial specification is 802.11, operated in the 2.4 GHz range and supports a maximum data rate of 1 to 2Mbps using a technology known as phase-shift keying (PSK) modulation. In late 1999, two new standards were released. The 802.11b specification adds two higher data rates of 5.5 and 11 Mbps in the 2.4 GHz range using Complementary Code Keying (CCK) [1, 2, 3] while the 802.11a specification is the standard for broadband communication systems and utilizes the5 GHz UNII band and supports data rates up to 54 Mbps The data rate can be changed with different coding rates according to the modulation type. The data is modulated with BPSK, QPSK, and 16/64QAM [3]. 802.11 g is a high data rate extension to 802.11 in the 2.4 GHz ISM band, and is compatible with 802.11 b. 802.11 g uses Orthogonal Frequency Division Multiplexing (OFDM) as radio transmission method, and supports four modulation formats (BPSK, QPSK, 16QAM, 64QAM) and convolution coding[8].

## III. BLOCK DIAGRAM

The general block diagram of the transmitter for OFDM based WLAN 802.11a is shown in fig.3 [5].

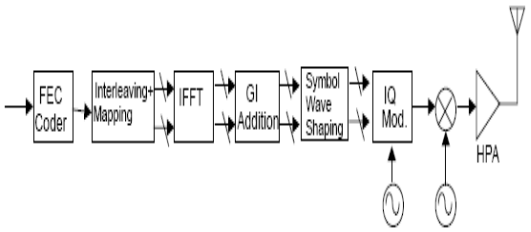


Fig. 3 WLAN (802.11a) transmitter [5]

Before transmission data is encrypted and encoded for secure and error free communication using Data scrambler and convolutional encoder. A scrambler is a device that transposes or inverts signals or otherwise encodes a message at the transmitter to make the message unintelligible at a receiver not equipped with an appropriately set descrambling device The Convolution Encoder core can be used in a wide variety of error correcting applications and is typically used in conjunction with the Viterbi Decoder. A block interleaver accepts a set of symbols and rearranges them, without repeating or omitting any of the symbols in the set. The number of symbols in each set is fixed for a given interleaver. The interleaver's operation on a set of symbols is independent of its operation on all other sets of symbols. An interleaver permutes symbols according to a mapping. A corresponding deinterleaver uses the inverse mapping to restore the original sequence of symbols. Interleaving and deinterleaving can be useful for reducing errors. Then 64 point IFFT has been performed which converts frequency domain to time domain [6, 7]. The required bandwidth of the transmitted signal is 20 MHz and the OFDM symbol duration is 4 us including 0.8 us for a guard interval. Thus, in effect, the IFFT operation has to be computed within 3.2 us without the guard interval. The OFDM subcarriers shall be modulated by using BPSK, QPSK, 16-QAM, or 64-QAM modulation, based on the RATE requested. The encoded and interleaved binary serial input data shall be divided into groups of $N_{BPSC}$ (1, 2, 4, or 6) bits and converted into complex numbers representing BPSK, QPSK, 16-QAM, or 64-QAM constellation points. By multiplying the resulting (I+jQ) value with a normalization factor KMOD, output values are formed,

d = (I + jQ) * KMOD.

The stream of complex numbers is divided into groups of $N_{SD}$ = 48 complex numbers. We shall denote this by writing the complex number dk,n, which corresponds to subcarrier k of OFDM symbol n, as follows:

$D_{k,n} = d_{k+ NSD * n}$, k = 0, ... NSD – 1, n = 0, ... NSYM – 1

The number of OFDM symbols, NSYM, An OFDM symbol, $r_{DATA},_{n(t)}$, is defined as[5]

$$r_{DATA,n}(t) = w_{TSYM}(t)\left(\sum_{k=0}^{N_{SD}-1} d_{k,n}\exp((j2\pi M(k)\Delta_F(t-T_{GI}))\right.$$
$$\left. + p_{n+1}\sum_{k=-N_{ST}/2}^{N_{ST}/2} P_k\exp(j2\pi k\Delta_F(t-T_{GI}))\right)$$

802.11a uses two sub bands, 5.15GHz to 5.35GHz and 5.725GHz to 5.825 GHz. Two sub bands together gives bandwidth of 300MHz, which is divided into 12 non overlapping data channels of 20MHz each [4]. XILINX Virtex performs the signal processing for 802.11a operation in Tx and Rx direction, e.g. interleaver, mapper, IFFT, insertion of guard interval [9].

## IV. IMPLEMENTATION

### IV.1 DATA SCRAMBLER

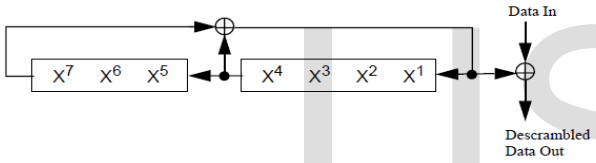


Fig.4 data scrambler [5]

The DATA field, composed of SERVICE, PSDU, tail, and pad parts, shall be scrambled with a length-127 frame-synchronous scrambler. The frame synchronous scrambler uses the generator polynomial S(x) as follows: S(x) = $x7+x^4+1$ [5] Scrambler and Descrambler use a shifting operation to introduce the delay in the data so as to obtain the required Cryptogram. X represents the delay operator (i.e. $x^N$ indicates the sequence is delayed by N units). The symbol '+' in the above equation represents modulo-2 addition [5]. For WLAN 802.11a, data is delayed by seven delay elements(flip flops). Outputs of 7th, 4th delay elements are modulo-2 added with 1 and gives scrambled data. Because seven data elements are used output is undefined for first seven clock pulses.

### IV.2 CONVOLUTIONAL ENCODER

The DATA, shall be coded with a Convolutional encoder of coding rate R = 1/2, 2/3, or 3/4, corresponding to the desired data rate. The bit denoted as "A" shall be output from the encoder before the bit denoted as "B. Higher rates are derived from it by employing "puncturing." Puncturing is a procedure for omitting some of the encoded bits in the transmitter thus reducing the number of transmitted bits and increasing the coding rate and inserting a dummy "zero" metric into the convolutional decoder on the receiver side in place of the omitted bits. [5].The convolutional encoder shall use the industry-standard generator polynomials, g0 = $(133)_8$ =$(1011011)_2$ and g1 = $(171)_8$ = $(1111001)_2$, of rate R = ½. Here A is the output of encoder after modulo-2 addition of input data, 2nd, 3rd, 5th and 6th delay element, based on 1011011. B is the output of encoder after modulo-2 addition of input data, 1st, 2nd, 3rd and 6th delay element, based on 1111001.

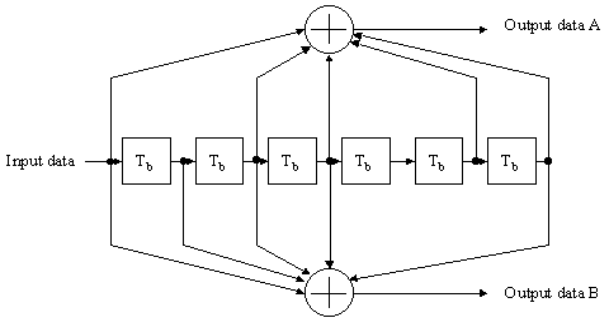


Fig.5 convolutional encoder [5]

### IV.3 DATA INTERLEAVER

In WLAN the interleaver is defined by a two-step permutation. The first permutation ensures that adjacent coded bits are mapped onto nonadjacent subcarriers. The second ensures that adjacent coded bits are mapped alternately onto less and more significant bits of the constellation and, thereby, long runs of low reliability (LSB) bits are avoided.

### IV.4 BPSK MODULATOR

In WLAN BPSK modulation is used for 6,9Mbps data rate, QPSK, 16-QAM, 64-QAM is used for higher data rates. From encoding table given below if input bit is 0 in phase component is -1 and quadrature component is 0 while if input is 1 in phase component is 1 and quadrature component is 0.

Table I. BPSK Encoding table

| Input bit | I-out | Q-out |
|---|---|---|
| 0 | –1 | 0 |
| 1 | 1 | 0 |

## V. SIMULATION RESULTS

### V.1 TRANSMITTER USING SIMULINK:

Software tools such as Matlab are used to model a complex, mixed-technology system prior to physically building and testing the system. These tools, along with their associated toolboxes provide an effective means for the initial modeling and simulation stages in a project. Such software tools also provide means to extract information in a

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relevant format to aid the physical realization. Hence WLAN transmitter is first simulated using MathWorks simulink and then same blocks are modeled in VHDL [10].

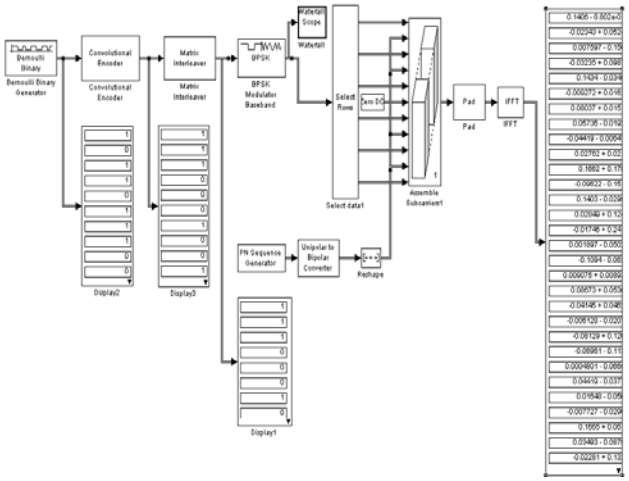

Fig.V.1.1 WLAN transmitter [5]

## V.2 TRANSMITTER USING VHDL:

### V.2.1 DATA SCRAMBLER:

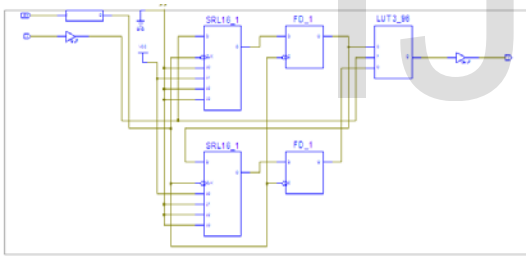

Fig V.2.1.1 RTL Schematic

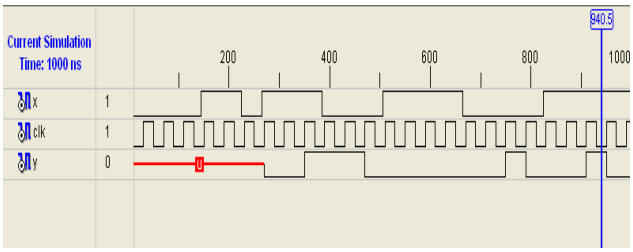


Fig V.2.1.2 Simulation Waveform

Table II. Resources Summary

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 2 | 6912 | 0% |
| Number of Slice Flip Flops | 2 | 13824 | 0% |
| Number of 4 input LUTs | 3 | 13824 | 0% |
| Number of bonded IOBs | 3 | 316 | 0% |
| Number of GCLKs | 1 | 4 | 25% |

### *V.2.2 Convolutional Encoder:*

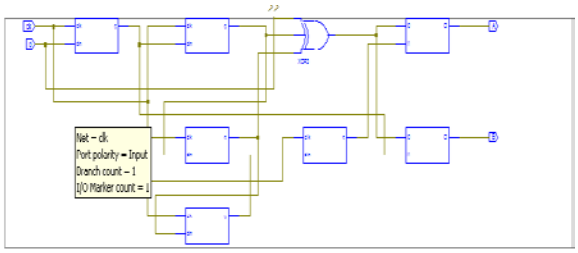


Fig V.2.2.1 RTL Schematic

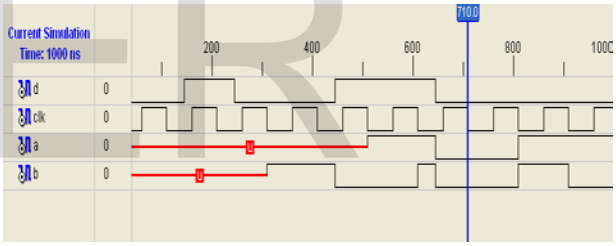


Fig V.2.2.2 Simulation Waveform

Table III. Resources Summary

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 2 | 6912 | 0% |
| Number of Slice Flip Flops | 4 | 13824 | 0% |
| Number of 4 input LUTs | 3 | 13824 | 0% |
| Number of bonded IOBs | 4 | 316 | 1% |
| Number of GCLKs | 1 | 4 | 25% |

### *V.2.3 Data interleaver:*

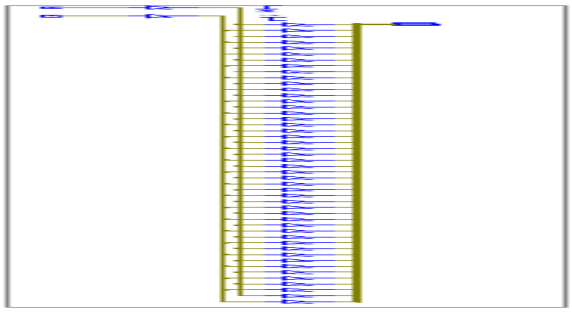

Fig V.2.3.1 RTL Schematic

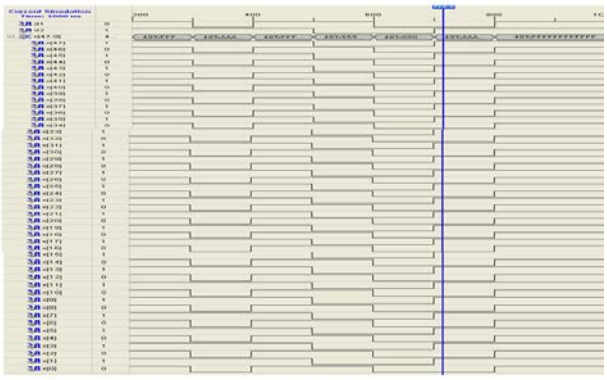

Fig V.2.3.2 Simulation Waveform

Table IV. Resources Summary

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 0 | 6912 | 0% |
| Number of bonded IOBs | 50 | 316 | 15% |

*V.2.4 BPSK Modulator*

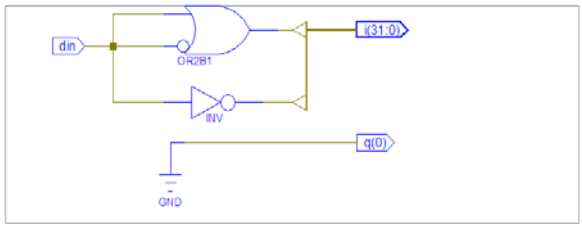


Fig V.2.4.1 RTL Schematic

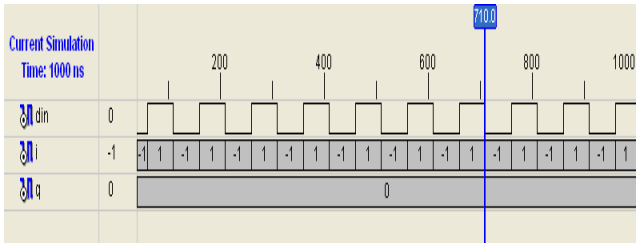


Fig V.2.4.2 Simulation Waveform

Table V. Resources Summary

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 1 | 6912 | 0% |
| Number of 4 input LUTs | 1 | 13824 | 0% |
| Number of bonded IOBs | 65 | 316 | 20% |

V.2.5 Inverse Fast Fourier Transform:

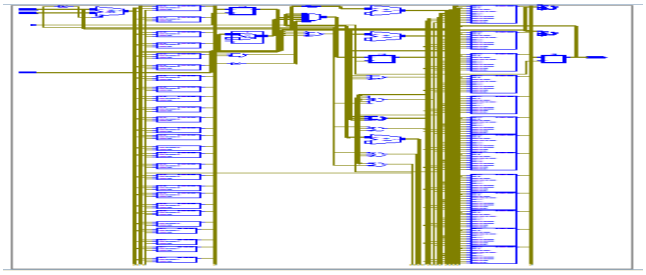

Fig V.2.5.1 RTL Schematic

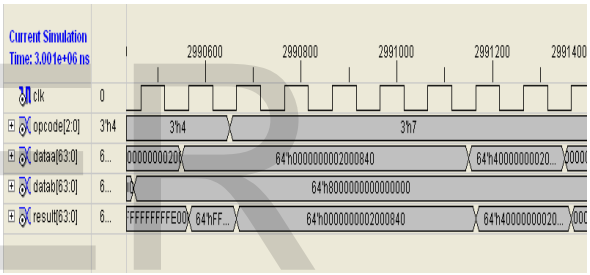


Fig V.2.5.2 Simulation Waveform

Table VI. Resources Summary

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 332 | 6912 | 4% |
| Number of Slice Flip Flops | 193 | 13824 | 1% |
| Number of 4 input LUTs | 606 | 13824 | 4% |
| Number of bonded IOBs | 196 | 316 | 62% |
| Number of GCLKs | 1 | 4 | 25% |

## VI. CONCLUSION

An OFDM prototype for the transmitter of IEEE 802.11a standard has been designed and simulated. Initial modeling and simulation is done using MathWorks simulink. The Study of different types of WLAN and simulation of IEEE 802.11a gave insight of diverse hardware requirements including processing speed, flexibility, integration and need for FPGA based implementation.

The transmitter is designed for 6 Mbps data rate with convolutional encoder been designed for coding rate of ½, BPSK as a modulation scheme, 64-point IFFT all the blocks were simulated using Xilinx ISE simulator. The synthesis

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results of individual blocks shows that the data scrambler utilize 2 number of slices out of 6912 which is 0% of available logic , 2 number of slice flip-flops out of 13824 which is 0% of available logic, Convolutional encoder utilize 2 number of slices out of 6912 which is 0% of available logic , 4 number of slice flip-flops out of 13824 which is 0% of available logic, BPSK modulator utilize 1 number of slices out of 6912 which is 0% of available logic, IFFT utilize 332 number of slices out of 6912 which is 4% of available logic , 193 number of slice flip-flops out of 13824 which is 1% of available logic of Xilinx Virtex xqv600e-6bg432.

The synthesis results using Virtex xqv600e-6bg432 shows that the FPGA platform gives flexibility when combining with other blocks, changing the design and adding new algorithms. The results also prove that use of FPGA platform saves area with less power dissipation leading to reduction in cost.

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